SOME DIAGNOSTIC PROPERTIES OF RECONFIGURABLE INTEGRATED CIRCUITS WITH BOUNDARY SCAN

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The paper presents a solution of the self-diagnostic problem of digital system by application of reconfigurable integrated circuits and boundary scan architecture. The implemented method of Built-In Self Test (BIST) is non-concurrent one and bases on the reconfiguration of the digital system, when the test mode has to be introduced. The author, with a microcontroller system as an example, shows an idea of improving the system diagnosability with minimum hardware overhead, by introducing reprogrammable gate arrays (FPGA) with modified functions, including adaptable BIST functions.

1. Introduction

Growing functional and structural complexity of modern digital systems, stimulates necessity of development effective Design-For-Test (DFT) techniques. They should ensure high level of the system diagnosability and reliability, and low level of extra cost overhead. Lately, the Boundary Scan Test (BST) architecture and method were introduced by IEEE 1149.1 Standard (Maunder and Tullos, 1990). According to the standard, digital systems could consist of integrated circuits with the BST subsystems inside each of them. The BST subsystems should be interfaced with the Test Bus (defined by 1149.1 Std.). Nowadays, there are on the market some IC's with standard functions and the BST subsystems built-in; system designers use also ASIC's, with the BST path inside them.

There is a question about DFT strategy, which should be used by a designer, who wants to built a diagnosable and reliable digital system for professional applications and small scale manufacturing. The author tries to answer the above question, using a microcontroller system as an example.

2. The Microcontroller With Boundary Scan Path

One of frequently utilised modules, that are used as elements of measurement or industrial automatic systems, is a local microcomputer controller (microcontroller), usually manufactured as a plug-in card, installed inside a cassette. In numerous applications there are needs for periodic or random self-diagnostics of the reliability states of the microcontroller and its elements.

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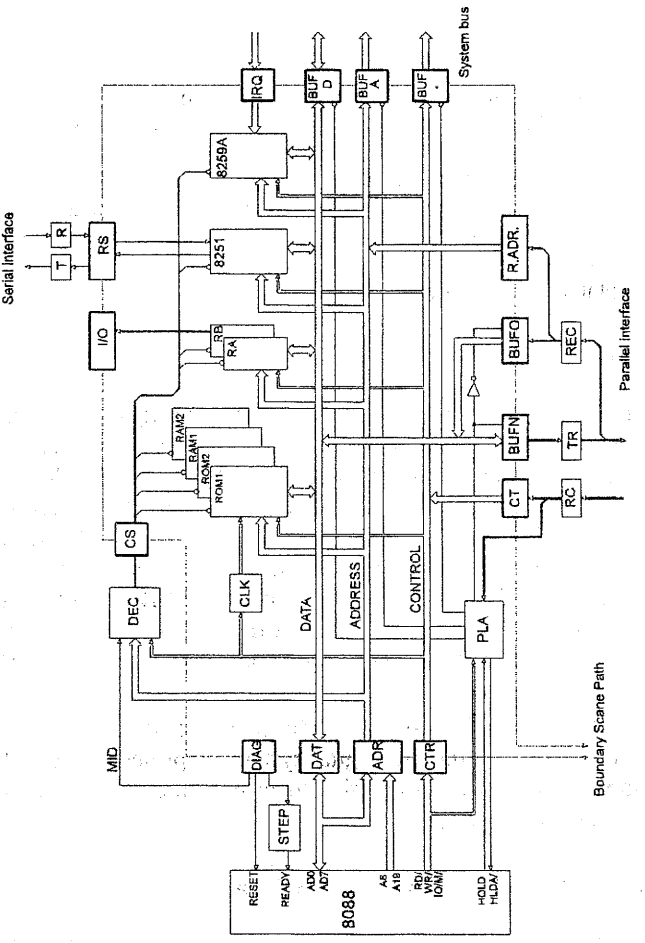

Fig. 1. Microcontroller board incorporating boundary-scan path.

The block schematics of such diagnosable microcomputer controller with application of Boundary Scan method and Test Bus, according to IEEE 1149.1 Std is presented in the Figure 1 (Adamkiewicz, Glinski and Lewandowski, 1992). There are elements, connected in the schematics with Test Bus (dotted line). These are "octals" SN74BCT8xxx, manufactured by Texas Instr. as equivalents of popular buffers (244, 245) and registers (374) (Morgan, 1990). Each of the octals is equipped with boundary scan subsystem, built according to IEEE 1149.1 Std . At normal operation of the controller, the octals perform its logic function in the digital system. In the Test mode of the system, the boundary scan subsystem in each "octal" is activated. The BST subsystems include test interfaces (called Test Access Ports - TAPs), test interface controllers (Test Access Port Controllers - TAPCs), instruction registers - IR, and a set of data registers - DR. The IR and boundary scan registers (connected with primary inputs and outputs of the octals) consist of BSR cells. Each BSR cell in each register stage possesses two memory elements - shift register element and shadow (latch) register element. The prototype of microcontroller from Figure 1 was built and verified with help of the Diagnostic Bus Analyser (Adamkiewicz, Glinski and Lewandowski, 1992), developed and manufactured in the PIE Institute. During design and execution of test-&-diagnostic procedures, there were some observations and conclusions obtained, described below in the paper.

3. Digital System Self-Testing With Pseudorandom Test Patterns and Signature Analysis

During testing a digital system with the BST method, there is a serious problem with transmission of large amount of test data (both input patterns and output responses). It could be omitted if the pattern generator and output data analyser would be installed in the IC's BST subsystem. In the "octals" SN74BCT8xxx, used in the microcontroller from Figure 1, Pseudorandom Pattern Generation (PRPG) and Parallel Signature Analysis (PSA) are performed by Linear Feedback Shift Registers (LFSR), configured with Boundary Scan Register cells (Whetsel and Young, 1990). To appreciate self-testing possibilities of inserting such "octals" in the digital systems, working with PRPG and PSA in test mode, the properties of these LFSR's were investigated.

The IC BCT8xxx could be configured for local self-testing in different three ways, determined by the state of a BCR (boundary control register) during RUNT instruction.

A. configuration with eight-bit, parallel input signature analyser on inputs of the IC (register R1), and eight-bit pseudorandom generator on the IC outputs (register R2); both registers R1 and R2 operate as independent Linear Feedback Shift Registers (LFSR);

B. configuration with two eight-bit registers R1 and R2 connected serially in one sixteen bit signature analyser with parallel eight inputs, connected to the inputs of BCT8244;

C. configuration with two eight bit registers R1 and R2 connected serially in one sixteen bit pseudorandom generator.

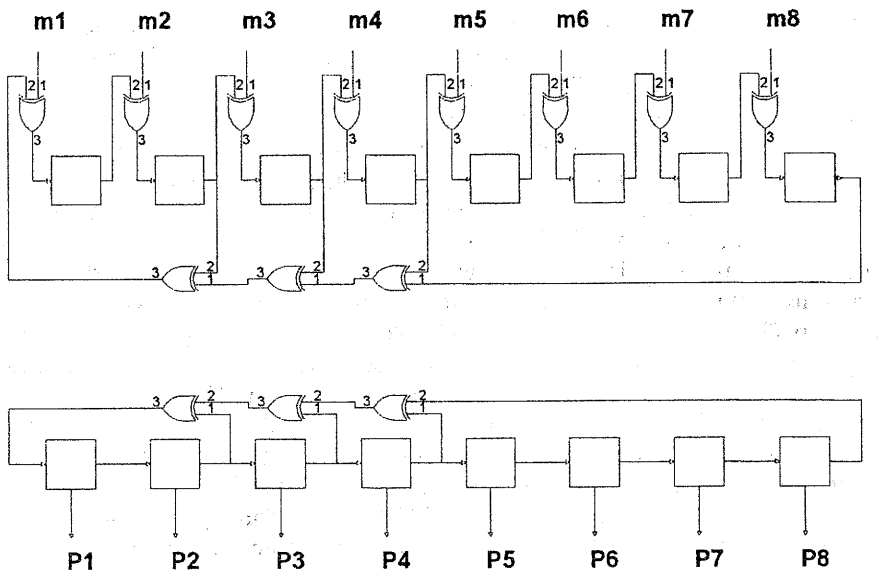

Fig. 2. The Linear Feedback Shift Registers obtained by a reconfiguration of the Boundary Scan Registers of the 74BCT82xx.

In all above three configurations, R1 and R2 LFSR registers could be modelled by primitive polynomial F(x) (Peterson, 1990):

$$F(x) = x^8 + x^4 + x^3 + x^2 + 1 \qquad (1)$$

General properties of sequences generated by LFSR's, determined by such primitive polynomials, are known. The number of different non-zero patterns is $2^m - 1$, if m is the number of flip-flops in the generator (in this case m = 8). When the PRPG stimulates a combinational circuit with r inputs, and r = m, the number of possible test patterns is equal 2^m. Then, for exhaustive test, the application of the PRPG is trivial in such a case. The problem is more complex if the number of primary inputs r of tested circuit is not equal m, (Nagrajara, Karpovsky and Levitin, 1991), or when the tested circuit is a sequential one. In such cases detailed analyses of the PRPG characteristics should be done for test procedure optimisation.

The characteristics of the polynomial F(x) could be determined by a numeric procedure, but for testing purposes author preferred computer simulation method. The model of the eight bit LFSR from Figure 2 was used in simulation process with SUSIE 6.0 simulator (ALDEC, 1990). The model could perform different functions on outputs P1÷P8, depending on input m1÷m8 states.

$$\text{If } mi = 0 \text{ for } i = 1,2,..,8, \text{ then} \qquad (2)$$

the model performs function of eight bit pseudorandom generator (PRPG) with serial input and parallel outputs P1÷P8. It generates so called M-sequence (Yarmolik, 1990).

$$\text{If } mi = yi \text{ for } i = 1,2,..,8, \tag{3}$$

(yi - output signals from elements of tested system), then the model performs function of a signature analyser MISR (Multi Input Shift Register - PSA) with eight parallel inputs.

$$\text{If } m1 = y1 \text{ and } mi = 0 \text{ for } i = 2,3..8, \tag{4}$$

then the model performs the function of the register R2 from C) configuration, or the function of eight bit signature analyser with serial input.

In the simulation process, the cases (2) and (4) were tested. The simulation results were generated as sequences s(n,i) - n bit long on generator output Pi, i = 1,2..8. The sequences were saved by simulator as ASCII files and then converted into digital matrix (spreadsheet).

$$s^i(n) = x_1, x_2, ..x_j, .., x_n \in Bn \; ; \; x_j \in B = \{0,1\} \tag{5}$$

To compare characteristics of different sequences, there were introduced some parameters of the sequences. The parameters base on the number of states "1" in particular sequences and segments, or on the number of state transition (transitions from high- to low state - "1\0"), as some measures of sequence uniformity.

The parameters are:

- "probability of '1' occurrence in a sequence", $p^1(s)$:

$$p^1(s) = \left\{ \sum_{j=1}^{n} x_j \right\} / n \tag{6}$$

- "probability of state transitions '1\0' in a sequence", $f^1(s)$:

$$f^1(s) = 2 * \left\{ \sum_{j=1}^{n-1} \left[x_j * \left(1 - x_{j-1}\right) \right] \right\} / n \tag{7}$$

The parameter $f^1(s)$ is counted as a number of one-directional state transitions "1\0", divided by the maximum possible number of state transitions, equal n/2 (n is the length of the sequence).

The probability $p^1(s^i_k)$ values were determined for eight lengths of the sequences- $n_1 = 32$, $n_2 = 64$, $n_3 = 96,...,n_8 = 255$. For n = 255, the probability $p^1(s)$ could be determined in numerical way, according to (Xilinx, 1991) as:

$$P^1(s(n)) = 1/2 + 1/(2^{n+1} - 2) \tag{8}$$

In the Figures 3 and 4 there are distributions of the probability of state transitions $f^1(s^i_k)$, counted for the same sequence points n_k, as above.

The files with output sequences P1÷P8, had obtained in the pervious simulation process, were used as a files with input data. In the Figures 5 and 6 there are presented characteristics for the PRPG in the configuration (4), when the PRPG is stimulated on its serial input by different sequences In_k.

The presented characteristics of the LFSR's, built in standard "octal" IC's with Boundary Scan, were useful for determination of parameters of self-test procedures for logic circuits with number of inputs less then 8, including sequential circuits of relatively small complexity.

The characteristics helped in determination of initial PRPG states, the test pattern length, and the selection of particular PRPG outputs for particular tested circuit inputs. The characteristics obtained for the 16-bit LFSR's configuration (Fig. 5, 6), show possibility of programming different probability distributions of pseudorandom patterns, and possibility of generation longer sequences of different test patterns than in the configuration (2).

There is another conclusion of the PRPG characteristics - limits of application the standard "octal" as a PRPG generator in cases, when optimisation of test procedures involves programming of the PRPG characteristics in greater limits, than limits achieved in the characteristics.

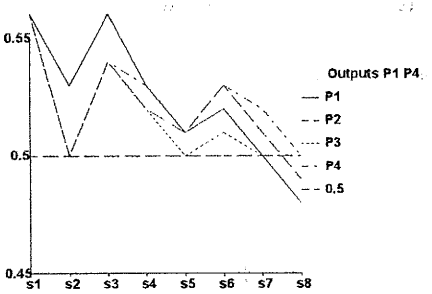

Fig. 3. Distribution of probability of state transitions (1\0), for P1-P4.

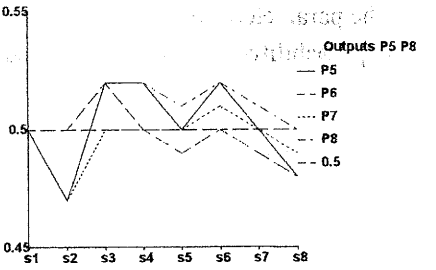

Fig. 4. Distribution of probability of state transitions (1\0) for P5-P8.

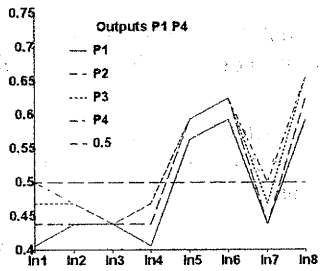

Fig. 5. Sequences P1-P4 as functions of input patterns In1-In8.

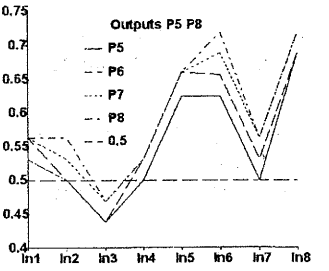

Fig. 6. Sequences P5-P8 as functions of input patterns In1-In8.

In these cases, application of standard octals (like BCT8xxx) could be inconvenient. Better results would be achieved with built in reconfigurable test pattern generators, with programmable architecture.

4. The Built-In-Self-Test System With Application of Reprogrammable Integrated Circuits

Difficulties with application of Built-In-Self-Test subsystems like pattern generators and test data analysers with universal structures are caused by great different demands for test procedures suitable for different kinds of digital circuits (combinational and sequential logic, memories, microprocessors, interface circuits). Optimisation of test procedures for each kind of diagnosed logic would be possible, when the BIST structures could be adapted to the particular needs.

There is a proposal to perform such adaptation of pattern generators or data analysers (compressors) with utilisation of reprogrammable gate arrays.

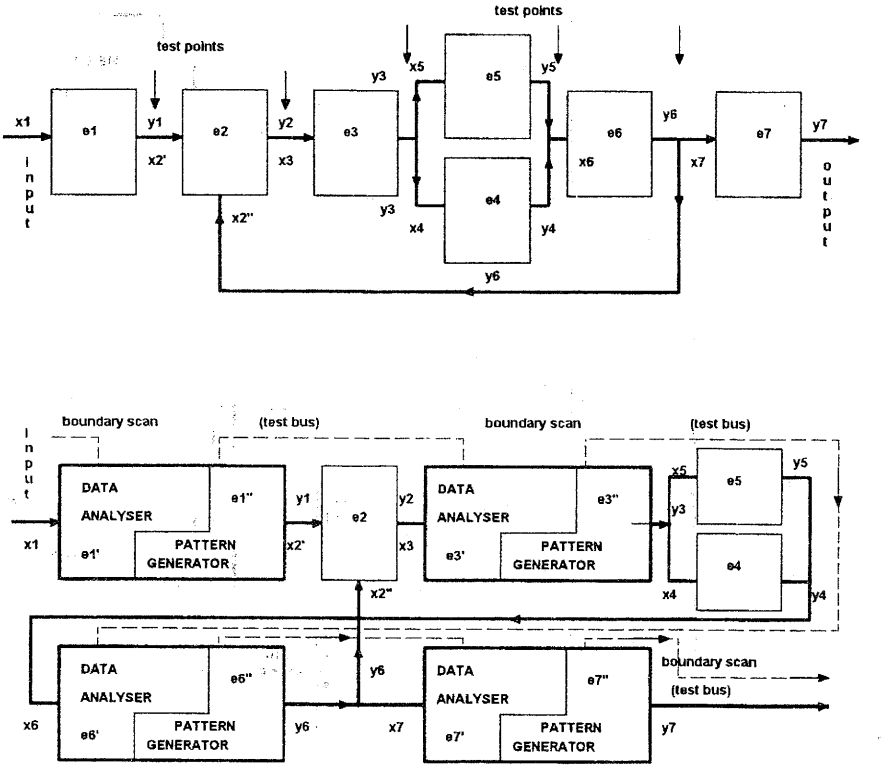

Fig. 7. An example of the system reconfiguration with programmable ASIC's (FPGA).

In the Figure 7 there is an example of a digital system with implementation of FPGA's as elements e1, e3, e6, e7. In the normal system operation, these elements function according to the digital system operation needs. In the test mode, the circuits e1, e3, e6, e7 are reconfigured to the test functions. The circuits are connected to the Test Bus, according to the IEEE 1149.1 Std.

In the Figure 8, there is a more concrete example - a subsystem consisting with e2, e3, e4, e5 blocks.

In the normal system operation, block e3, implemented with FPGA integrated

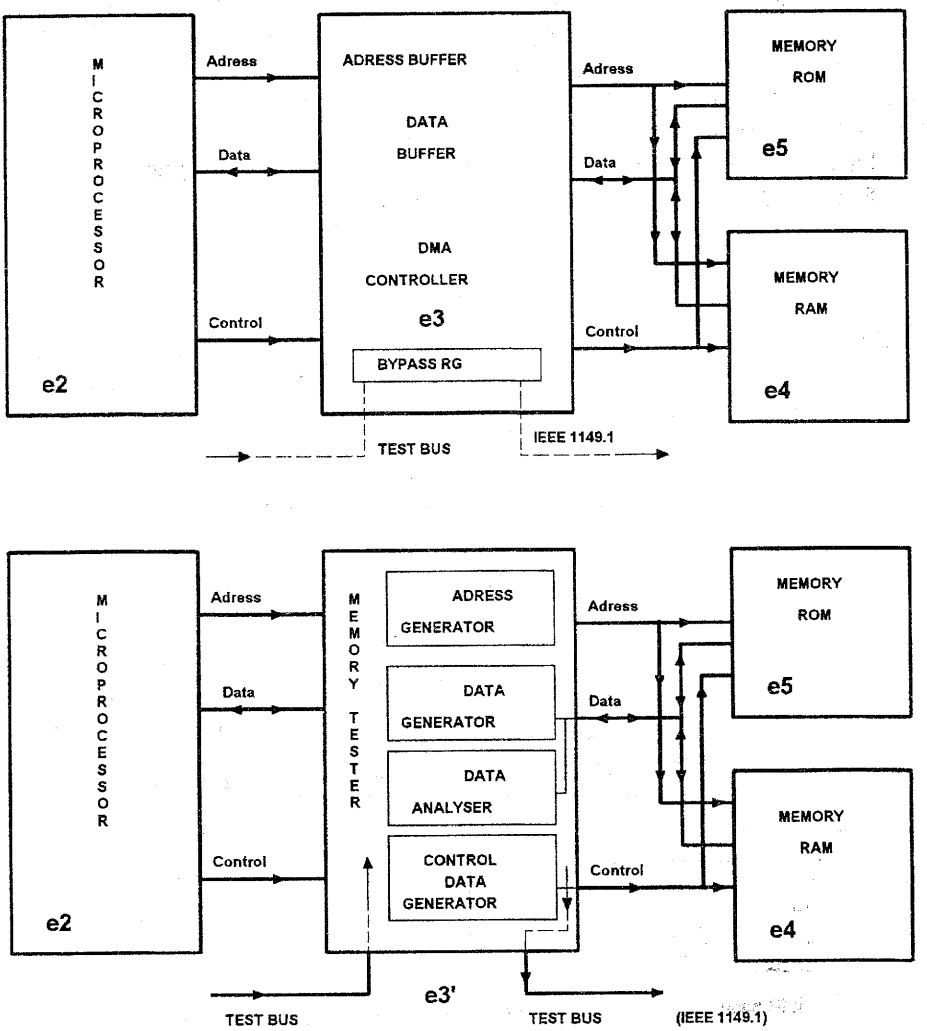

Fig. 8. An example of the element e3 reconfiguration from a data buffer and DMA controller to a memory tester.

circuit (or circuits), performs address and data buffer functions and works as a DMA controller. During the first test mode e3 is reconfigured to e3' and performs memory tester functions.

Memory tester consists of address, data, control signals generators and data analyser.

During the second test mode, the e3 block (or e3') is reconfigured once again to the e3" block-to the microprocessor tester.

In this case, e3" consists of address analyser, data generator/data analyser and

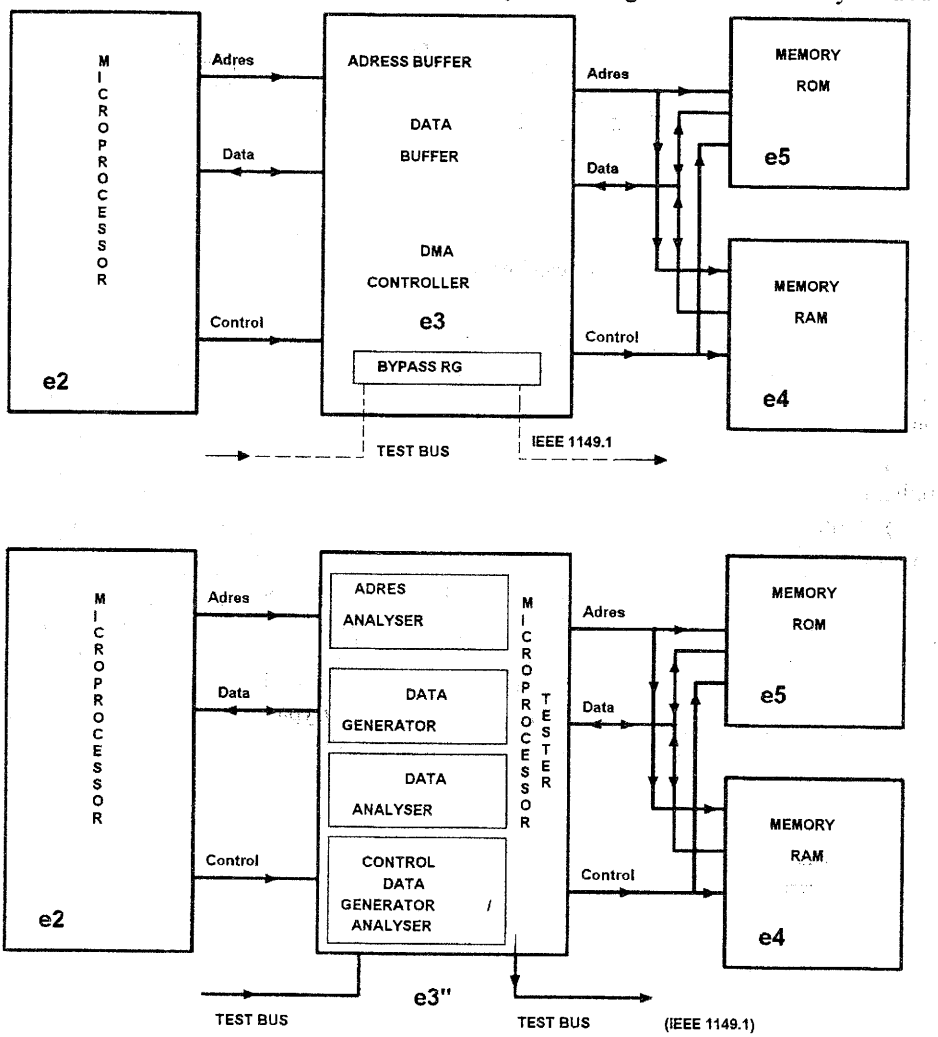

Fig. 9. An example of the reconfiguration of the e3 element to a microprocessor tester.

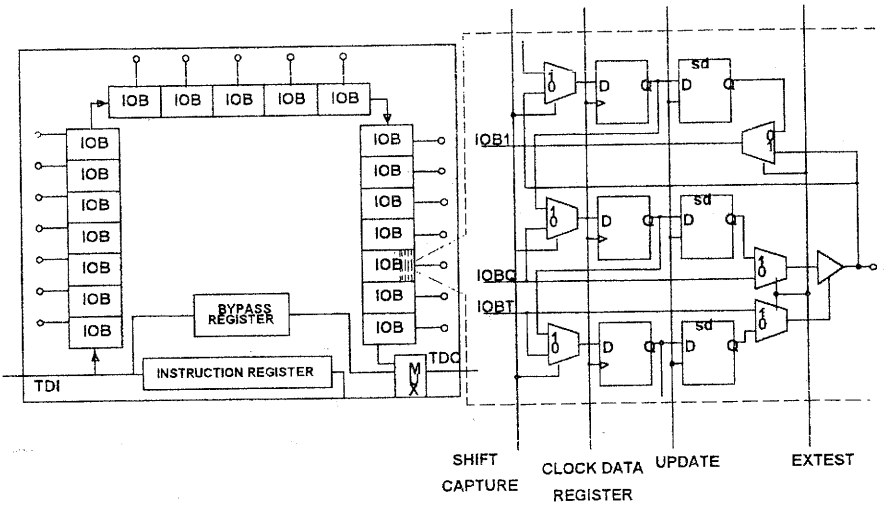

Fig. 10. The Boundary Scan Testing subsystem, created in XC4000.

control data generator/analyser. In every case, the generators and analysers could be adapted to the needs of test engineers. The BIST structures could be optimised from the point of view of maximum fault coverage and minimum cost of implementation. Of course, the optimisation should be performed in the limits, determined by technology.

The physical implementation of the presented idea could be performed with application of

XC4000 Xilinx reprogrammable gate arrays. The XC4000 family could be programmed to the Boundary Scan architecture, according to the IEEE 1149.1 Std. In the Figure 10 there is presented a schematic of the BST subsystem, implemented in the XC4000 FPGA circuit (Xilinx, 1991).For each IOB pin, there is a set of three bits of shift registers and three "update" registers for input, output and three-state mode control. The IOB registers are linked as a Boundary Scan Register. There are two special registers, according to IEEE 1149.1 Std: one-bit Bypass Registers and three-bit Instruction Register. The codes of instructions are as follow:

000 EXTEST
001 SAMPLE
010 USER1
011 USER2
100 reserved
101 reserved
110 reserved
111 BYPASS

It is possible to implement two special "user's" instructions: USER1 and USER2. The instructions could be involved in some BIST structures and BIST operations (as

shown in the above examples). There is available the special data register clock (BSCAN.DRCK) which could be implemented for synchronising the BIST structures during test operations.

5. Conclusions

Main advantages of the self-diagnostics with help of the reprogrammable the FPGA ASIC's are as follows:

- there is no need to built the BIST special hardware in the system; in the testing mode we can use the same hardware elements for diagnostic, as we use for normal system operation.
- during diagnostic process we can adapt the configuration of testing blocks (pattern generators and data analysers), according to the characteristics of the tested element; in further steps of diagnostics the configuration could be changed several times.

The main problem which should be solved in the further works, it is the design a set test procedures and BIST architecture models, suitable for different kind of clusters and VLSI modules. These structures, of course, should be introduced into XC4000 library.

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