WORKING PARTY 1: ASIC DESIGN, CAD TOOLS & METHODOLOGY

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A working party has been assembled, comprising academics from the six original participating institutions in JEP 0449, to suggest the curriculum for a course in 'ASIC Design, CAD Tools and Methodology' at the Polish institutions of Wroclaw Technical University and Zielona Gora Higher College of Education. The working party has identified the time that is available for the course at each of the institutions, assumed to be about 120 hours total, and has recommended lecture content and practical activities. The four sections of lectured material are 'Digital System Design', 'ASIC Implementation Styles', 'Computer-Aided Design' and 'Testing'. Initially, practical activities are to concentrate on programmable devices including conventional Programmable Logic Devices (PLD) for simple exercises and, to mimic as closely as possible the environment of a conventional mask-programmable gate array, Xilinx Logic Cell Arrays (LCA) for more demanding projects. Exercises are to include schematic capture and hardware description languages (including VHDL), logic simulation, layout, implementation and testing of designs.

1. Introduction

Tempus contract JEP0449, 'Advanced Computing Education Project', involving the University of Bristol (England), University of Aveiro (Portugal), University of Minho (Portugal), UMIST (England), Wroclaw Technical University (Poland) and Zielona Gora Higher College of Education (Poland), was announced in December 1990 and the management committee held its first meeting in February 1991. At this meeting the composition of three working parties, 'ASIC Design, CAD Tools and Methodology', 'Advanced Computer Architecture' and 'Equipment Purchase', was decided. The working party for the present activity, consisting of Dr. Trevor York (UMIST, Chairman), Professor Marian Adamski (Zielona Gora), Dr. Dariusz Caban (Wroclaw), Professor Antonio Ferrari (Aveiro), Dr. David Milford (Bristol) and Professor Alberto Proenca (Minho), has since met on three occasions to discuss course content.

An extract from the original proposal gives some indication of the intended scope of the course and it is perhaps worth considering this and later comparing it to the achievements so far :

"The course in ASIC design is in response to the rapid developments occurring in integrated circuit design and fabrication. The course will cover the core material

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needed to enable engineers to specify, design, simulate, layout, test and fabricate Application Specific Integrated Circuits. It is expected to relate very closely to the VLSI Design Skills Initiative (EUROCHIP) currently being funded under an ESPRIT programme."

The initial management meeting identified terms of reference for the working parties as follows :

1. Define the range and scope of the syllabus.
2. Consider teaching patterns in each institution.
3. Set objectives for preparation of teaching material : lectures, practicals, projects, examples classes.
4. Identify pre-requisite and complementary courses.
5. Recommend suitable textbooks
6. Report equipment requirements to the Equipment Working Party.

Armed with these guidelines the working party embarked upon the task of formulating the structure of a course on 'ASIC Design, CAD Tools and Methodology'. The original proposal for the JEP had suggested that this course should occupy a total of 4 hours per week for 1 semester in the timetable.

The remainder of this paper presents an account of the considerations that have arisen, at meetings of the working party, while formulating proposals for the course. It outlines the perceived objectives of the course, considers existing material, in each of the participating institutions, and its relevance. Lecture course content and practical activities are suggested and a summary is given of achievements so far together with projected activities for the future.

2. Objectives of the Course

The working party has identified a mission for the course, as follows :

To enable students to undertake the design of a digital system from high level specification through to implementation using appropriate ASIC technologies

In order to avoid confusion at a later stage it is perhaps advisable to consider the term Application Specific Integrated Circuit (ASIC). First introduced about eight years ago, when it was primarily applied to mask-programmable semi-custom integrated circuits, principally gate arrays and, more latterly, cell-based chips, it is now applied to a variety of design styles. In recent years the distinction between different styles has become increasingly vague, especially regarding the complexity of devices and suitability for specific applications. This is largely as a result of the introduction of the Field Programmable Gate Array (FPGA) in about 1985. For this reason, for the present purposes, it is intended that the term ASIC embraces both mask-programmable and field-programmable custom integrated circuits, including full custom, gate array, cell-based, FPGA and conventional Programmable Logic Devices (PLD), as typified by the PAL.

It was agreed at an early stage that, considering the interests and experience of the Polish institutions and also due to the considerable demands on hardware and software

resources, for the present full custom VLSI design should be excluded from the syllabus. It was agreed that it could be considered as an option when the course has had a chance to mature, providing that sufficient resources were available to finance the activity.

3. Existing Courses Relating to 'ASIC Design, CAD Tools and Methodology'

At the first management meeting representatives of each of the academic participants suggested figures for their present teaching commitment, related to this activity, as indicated below.

Table 1. Existing related activities at the participating institutions.

Institution	Course	Year	Lectures	Practicals
Aveiro	LEE	3	30	15
	LEE	5	15	15
Bristol	EE/CSE	2	30	15
	EE/CSE	3	15	15
Minho	LESI	2	20	14
UMIST	EE/MSE	2	20	9
	EE	3	20	6
	MSE	3	20	30
	MSE	4	25	25
	VLSI	MSc	30	50
Wroclaw	CSE/EE	3	25	20
Zielona Gora	DS	3	15	45
	DS	4	20	45

Students of Computer Engineering in the Department of Electronics at Wroclaw and Computer Science and Metrology in the Department of Electrical Engineering at Zielona Gora attend for 10 Semesters, each of 15 weeks duration, for a period of 5 years.

3.1. Overview of the Computer Engineering Course at Wroclaw

For the first four semesters the material is common to all students, essentially comprising fundamental mathematics, electronics and computer science, but after this increasing attention is paid to the chosen specialisation, leading to M.Sc., in either 'Computer Systems and Networks' or in the present case 'Microprocessor and Microcomputer Systems'.

Topics included in the latter specialisation include :

Architecture and Programming of Microprocessor Systems

Programming Languages and Systems

Microprocessor Systems Design and Diagnostics

Microcomputer Operating Systems

Computer Graphics

Computer systems modelling Methods

Fault tolerant Circuit Design

Distributed Systems

Computer Networks

From the existing material the following was felt to be of direct relevance to the proposed course in 'ASIC Design, CAD Tools and Methodology' :

Semester III : Semiconductor theory

Semester IV : Introduction to Digital Design and Microprocessors

Semester V : Digital Devices and Circuits

Semester III, IV : Automata Theory

Each of these courses is presently taught as part of the core material in Computer Engineering.

The proposed course has been scheduled for semesters VIII and IX and will occupy 4 hours per week resulting in an overall total of 120 hours. It is estimated that between 30 and 40 students per year will attend the course.

3.2. Overview of the Course in Computer Science and Metrology in Zielona Gora

The course is split into 36 modules and again, early material covers basics, concentrating on mathematics, physics, electrical and electronic engineering and computer programming. The latter part of the course extends into areas that are more directly related to the present JEP including :

Electronic Digital Circuits

Computer Networks

Computer Architectures

Object Oriented Programming

Advanced Programming Techniques

Principles of Artificial Intelligence

Microprocessor-Based Measurement Equipment

In particular, the present material is to be presented in module 29, 'Computer-Aided Design of Digital Systems' in semesters VI, VII and VIII, comprising about 150 timetabled hours of activity. About 15 to 20 students per year are anticipated for the course.

Existing material of direct relevance to 'ASIC Design CAD Tools and Methodology' is covered in the following modules:

Semesters IV, V : module 22 : 'Electronic Digital Circuits'

Semester V : module 14 : 'Electronic Circuits'

Semester V : module 16 : 'Electrical Devices'

4. Proposed Course in 'ASIC Design, CAD Tools and Methodology'

At its first meeting the working party considered the relevant patterns of teaching in each of the participating institutions. It was finally agreed that a course duration of 120 hours should be assumed, twice that suggested in the original proposal, with twice as much time devoted to practical work compared to lectures.

4.1. Lecture Material

After some debate it was felt to be of primary importance that the course should convey the benefits of a top-down approach to design and, while recognising the need for the fundamentals of logic design, should encourage a realistic modern approach, in terms of CAD tools, for undertaking such tasks. It was recognised that, while it was common to find strong support for teaching specification and behavioural description for the early stages of design, this aspect was often included in the latter parts of courses.

Table 2. Proposed sections in 'ASIC Design, CAD Tools and Methodology'.

Digital System Design (16 hours) Top-down approach, Specification, Behavioural Description, System Partitioning, Algorithmic State Machine, Structural Description
ASIC Implementation Styles (8 hours) The Need for ASICs, Comparison of Off-the-Shelf, Mask Programmable and Field Programmable approaches
Computer-Aided Design (8 hours) Schematic Capture, Simulation, Layout, Minimisation tools, Hardware Description Languages, Frameworks, Data Interchange, Introduction to Formal Verification, Automatic Synthesis
Testing (8 hours) Testing ASICs, Design for Test, Built-In Self-Test, Test Pattern Generation, Boundary Scan, Fault Simulation

Therefore the working party strongly advocates the inclusion of such topics in the early part of the course. The proposed lecture content was split into four sections as indicated in table 2 together with suggested outline syllabuses. The approximate duration of each section is included in brackets. Central to the course and of fundamental importance is the section on 'Digital System Design'.

The lectures will assume certain prerequisite material as suggested below. Logic Design is presently covered at both institutions while Silicon Technology is only covered at Wroclaw.

Table 3. Prerequisite material for 'ASIC Design, CAD Tools and Methodology'.

| **Logic Design** |
| Boolean Algebra, Combinatorial Logic, Truth Tables, Karnaugh Maps, Sequential Logic, Introduction to State Machines |
| **Silicon IC Technology** |
| Silicon Fabrication, Bipolar and MOS Processes, Logic Families |
| (not currently at Zielona Gora) |
| **Introductory CMOS Design (Optional)** |
| DC and Transient Switch Level Analysis of Basic nMOS and CMOS Gates, Static and Dynamic CMOS, Transmission Gate Logic, Input Protection, Latch Up, Sequential Logic Structures, PLA, RAM and ROM |

4.2. Practical Activities

Ideally the course should expose students to the complete cycle of a mask-programmable custom chip, from specification, through design, to fabrication, implementation and testing. As discussed earlier, full-custom design was considered to be outside the scope of discussions for the present time and therefore conventional gate arrays and cell based designs were felt to be of most relevance. For mask-programmable design the following observations should be considered:

   i) PC-compatible machines are barely adequate for anything other than trivial teaching exercises.

   ii) Workstations are more expensive than PC-compatible machines.

   iii) The necessary CAD tools for mask-programmable design are expensive.

   iv) Fabrication of mask-programmable chips is typically very expensive, unless initiatives such as UK ECAD or EC VLSI Design Skills are available.

   v) Fabrication introduces undesirable delays into practical exercises.

Considering the existing facilities at Wroclaw and Zielona Gora together with those that are anticipated in the near future, as a result of Tempus and other initiatives, it is recommended that practical work should concentrate on field programmable

devices. Some of these offer an environment that closely resembles that of the mask-programmable approach, while incurring no great component cost or 'time-to-testing', and are entirely practical using a PC-compatible host. It is important to teach respect for first-time correct design, especially regarding mask-programmable ASICs. Therefore it is highly desirable that the chosen design route, for field-programmable devices, conveys the importance of thorough design verification in achieving this aim and the choice of preferred technology will be strongly influenced by this consideration. It should be emphasised that the above considerations, while appropriate for many teaching situations, should not undermine the importance of mask-programmable ASICs in the commercial world.

The exercises should embrace schematic capture, Hardware Description Languages (HDL), logic simulation, layout, implementation and testing. Discussion took place during the meetings regarding the vehicle for teaching HDLs. While it was acknowledged that VHDL is the recognised tool, worldwide, some reservations were expressed regarding its suitability, especially as it necessitates considerable training. Some support was voiced during the meetings for using a high level programming language, such as Pascal, as this could convey the important principles involved. The inability of such an approach to simulate concurrent processes was felt to be a limiting factor.

Proposals for the practical work, comprising 80 timetabled hours of activity, are given below :

    i) Introductory exercises for schematic capture and simulation (20-35 hours)

    ii) Introduction to HDL (6 hours)

    iii) Simple state machine/sum-of-products design using a PLD (9 hours)

    iv) More complex 'system on silicon' design project using a Programmable Gate Array (30-45 hours)

    v) Tutorials (15 hours)

4.2.1. Programmable Logic Device (PLD) Design

Conventional PLDs, as typified by the PAL, are readily available and inexpensive and therefore it is, perhaps, most important to consider the tools that are available for designing such devices. The recognised industry leaders are ABEL, from Data I/O, costing about £2K and CUPL, from Logical Devices, costing about £1.7K. Both of these tools offer the ability to program a wide selection of devices from many different vendors. In contrast PALASM, costing only £100, is specific to the vendors AMD. All of these tools include a basic HDL for design entry and this can be in the form of Boolean equations, truth table or a state machine language. CUPL was selected as the preferred tool as it offers more flexibility than PALASM and was more familiar to members of the working party than ABEL. Erasable chips are available for as little as £1 but more typically £5. Implementation of PLD based designs requires a programming tool which typically consists of a plug-in card for the PC and a module incorporating a socket. Such programmers are available for as little as £500 but can cost £10K.

4.2.2. Programmable Gate Array Design

Since about 1985 a type of device called the Field Programmable Gate Array (FPGA) has been available from a number of companies. Such devices typically offer increased functionality, in terms of equivalent 'gates', compared to conventional PLDs, to levels approaching those to be found on modest, mask-programmable, gate arrays. The FPGAs vary mainly in architecture and method of programming. At one extreme FPGAs comprise regular, two-dimensional, arrays of simple cells, each having the complexity of a small NAND gate. At the other the chips include a small number of larger, 'PLD' type modules, each comprising of a number of 'PAL' type macrocells, offering, latched, sum-of-products expressions. Programming techniques vary, from volatile, embedded RAM, through EPROM technology to 'one-shot' methods using specially fabricated antifuses. Table 4 summarises some of the more popular types of FPGA that were considered for the present course. The devices mentioned in the table vary from those resembling conventional gate arrays at the top to those with a coarser architecture, often called complex PLDs, and resembling multiple PALs, at the bottom.

PC-based FPGA design routes that were considered are summarised in Table 5.

Marketing of the Plessey devices is now managed by Fujitsu but little is known of the supporting software. Design routes for all the FPGAs are similar, typically involving schematic capture and simulation, using third party software, followed by layout **using proprietary CAD tools**. It is also possible to describe a FPGA using a simple HDL, similar to those encountered for PLD design, however in order to provide a contrast, it was felt that a route involving schematic capture was to be encouraged. In discussing the possibilities with the vendors it would seem that a PC-based route is preferred. The routes involving ACT, MAX and MACH devices require special

Table 4. Programmable Gate Arrays.

TYPE	MAXIMUM 'GATES'	CHIP COST	PROGRAMMING METHOD	BASIC CELL
PLESSEY ERA	2.5K (10K)	???	Embedded RAM	NAND2
ACTEL ACT	8K (16K)	£15 (1K) £30 (2K)	PLICE antifuse (1 shot)	NAND 4
XILINX LCA	9K (20K)	£10 (1K) £50 (4K)	Embedded RAM	NAND 5 LATCHED
ALTERA MAX	8K (20K)	£15 (700) £30 (2K)	EPROM	'PAL'
AMD MACH	1K (4K)	£15 (1K)	EPROM	'PAL'

Table 5. PC-based CAD tools for PGA design.

TYPE	SCHEM. CAPTURE SIMULATION	'LAYOUT'	HDL APPROACH
ACTEL ACT	VIEWLOGIC	ACTEL ALS	ABEL FPGA,
XILINX LCA	VIEWLOGIC ORCAD	XILINX XACT	ABEL FPGA
ALTERA MAX	ALTERA MAX+PLUS II VIEWLOGIC	MAX+PLUS II	MAX+PLUS II
AMD MACH	ORCAD PLD	PALASM ABEL 4, CUPL	PALASM ABEL 4, CUPL

programming tools. It should be noted that ABEL FPGA is an enhanced and consequently more expensive tool than ABEL 4 which is suggested for PLD design. Sample prices of typical software combinations are shown in table 6. It should be noted that these figures reflect commercial prices and that, in most cases, considerable reductions should be negotiated for educational purposes.

Table 6. Typical CAD costs for FPGA design.

Actel ACT	
Viewlogic, ALS, Actel programmer	£5K
ABEL FPGA, ALS, Actel programmer	£9K
Altera MAX	
Viewlogic, MAX+PLUS II, MAX programmer	£9K
Altera+Plus II, MAX programmer	£7K
Xilinx LCA	
Orcad, XACT, EPROM programmer	£4.5K
Viewlogic, XACT, EPROM programmer	£6.5K
AMD MACH	
PALASM, PAL programmer, adapter	£1K

    From the considerations described above it was possible to identify preferences. Ideally, for maximum flexibility in design, the students should be exposed to a conventional gate array environment comprising simple cells. For this reason the Altera MAX and AMD MACH chips were rejected. Members of the working party were unfamiliar with the Plessey ERA devices but felt that the software was not impressive.

Of the two remaining devices, namely Xilinx LCA and Actel ACT, the latter was preferred as it most closely resembles the mask-programmable approach although it does incur a recurring component cost as the chips can only be programmed once. Xilinx LCAs are well known to the working party and, while offering a suitable architecture, do not discourage poor design techniques as they are readily re-configured with negligible penalty. In addition they offer volatile solutions which are not strictly 'single chip'.

Considering the above, it may be worthwhile to consider a possible scenario that may be encountered by a fresh graduate in a hi-tech company. Assume that this graduate is asked by the manager to recommend the most suitable route for a design comprising about 20K 'gates' which is expected to realise about 1000 sales. For a cell-based design the 'tooling' or Non Recurrent Engineering (NRE) charge may be about £20K. The necessary silicon for 1000 chips may cost about £2K and packaging may be £1 per chip. This results in a cost of £23 per chip compared to something greater than £100 for a FPGA approach (which would also require more than one chip). Obviously the cell-based approach is preferred. The key point is that, for the manager to proceed with confidence, it is desirable that the graduate has experienced a design route that is as close as possible to that for mask-programmable design. In particular the grave consequences of any mistakes and the importance of 'first time correct' design must be appreciated. Among the FPGA routes Actel is nearest to this environment. Some caution must be recommended for the Xilinx approach in which the effort required to realise thorough simulation is not easy to justify.

The working party recommended Actel ACT chips as the vehicle for teaching 'gate array' type design and as the basis of a 30-45 hour project. Viewlogic, recognised as perhaps the leading PC-based CAD package, was originally recommended as the front end of the design route. Unfortunately, despite having identified 'ideals' as described above, practical considerations then took precedence. Due to insurmountable difficulties in acquiring Viewlogic in Poland, the proposal to use Actel had to be abandoned in favour of Xilinx with Orcad.

4.2.3. Testing

Following implementation it is desirable that students are able to test their designs. At present there are no suitable facilities available at either institution and therefore this aspect has not been extensively discussed. Considering that the present activities are PC-based it is unlikely that any facility will be capable of anything other than the most routine test, however a test route is highly desirable. ASICMASTER is one example of low-cost ATE, available in England for about £12.5K, that is used in conjunction with a PC and could offer functional testing but is unlikely to be fast enough to yield results on timing. There is currently no provision in the JEP budget for such equipment.

4.3. Recommended Textbooks

One other task for the working party is to recommend textbooks for the course. The suggestions are listed below according to the sections suggested for the lecture material.

Digital System Design :

Bolton M, 'Digital Systems Design with Programmable Logic', Addison-Wesley, 1990, £21-95 (ISBN 0-201-14545-6).

Green D.H, 'Modern Logic Design', Addison-Wesley, 1986, £19-95 (ISBN 0-201-14541-3).

Perry D, 'VHDL', McGraw Hill, £34-95 (ISBN 0-070-49433-9).

Wakerley J.F, 'Digital Design Principles and Practice', Prentice Hall, 1990, £19-95 (ISBN 0-13-212879-9)

Winkel and Prosser, 'The Art of Digital Design', Prentice-Hall, £16-95 (ISBN 0-130-46673-5).

Asic Implementation Styles :

Morant M.J, 'Integrated Circuit Design and Technology', Chapman and Hall, 1990, £11-95 (ISBN 0-412-34220-0).

Hurst S, Custom VLSI Microelectronics, Prentice Hall, 1992, £45-00 (ISBN 0-13-194416-9).

CAD :

Rubin S, 'Computer Aids for VLSI Design', Addison-Wesley, 1987, £29-95 (ISBN 0-201-05824-3).

Russell G, CAD for VLSI System Design, Peter Peregrinus, 1987, £14-95 (ISBN 0-442-30618-0).

Testing :

Bennetts R.G, 'Design of Testable Logic Circuits', Addison-Wesley, 1984, £18-95 (ISBN 0-201-14403-4).

Wilkins B.R, 'Testing Digital Circuits', Chapman and Hall, 1986, £15-95 (ISBN 0-412-38360-8).

5. Status of Course Development

Associated with this project the two Polish institutions have each received PC-compatible computers, Orcad for schematic capture and simulation, CUPL, VHDL and a PLD programmer. Wroclaw have received the Xilinx layout software, XACT, and arrival of the copy for Zielona Gora is imminent. The version of VHDL is felt to be, perhaps, rather basic and in particular the documentation is almost non-existent.

Regarding the taught material, some delays have been experienced due to a number of factors. Perhaps of most significance is that the personnel who are mainly responsible for course development in each institution have been involved in staff mobility associated with the JEP. Secondly, although textbooks were recommended at an early stage, no formal decisions were made to purchase these books for the teachers. Understandably this has lead to some reluctance to embark on new material. Some progress has been made at Zielona Gora where new material associated with Digital Systems Design, in particular relating state machine design to HDL description, has

been introduced. In addition, practical exercises using Orcad for schematic capture and simulation and PALASM 2 for PLD design have been undertaken by the students. The decision to use PALASM rather than CUPL, which was recommended by the working party, was based on its simplicity and the fact that AMD allow multiple copies to be used concurrently. For this reason the working party has recommended the purchase of PALASM 4 for class exercises with CUPL reserved for more demanding project work. Another factor that has been overlooked is that some difficulties may be experienced in acquiring chips to support these activities and this should be explicitly addressed by the JEP. A laboratory script for CUPL has been prepared during the visit of a member of staff from Wroclaw to England. The introduction of new material at Wroclaw will begin at the start of the new academic year in October.

6. Summary and Future Directions

This paper presents details of the proposals for a course in ASIC Design, CAD Tools and Methodology' at Wroclaw Technical University and Zielona Gora Higher College of Education as part of Tempus JEP 0449. The proposed course should satisfy many of the original aims, regarding exposure of students to the complete ASIC design cycle, however its relationship to the EC VLSI Design Skills initiative is tenuous as the proposals presently exclude any mask-programmable ASIC design and comprise entirely PC-based activities. One outstanding problem at the moment concerns testing as there is presently no route available at either institution.

It has become apparent that the original objectives regarding the introduction of material to the curriculum failed to acknowledge the impact of staff mobility associated with the JEP and this has lead to some delays in preparation. In addition the failure to ensure that at least one copy of each recommended textbook was purchased for each institution has also caused difficulties. Similarly, unless chips are explicitly provided via Tempus, practical activities may not be able to realise working prototypes.

With the gradual introduction of workstations it should be possible, at some time in the future, to consider mask-programmable design, eventually including full custom design, possibly as an option. This suggestion acknowledges the need for extensive negotiation regarding software procurement and fabrication costs, if facilities such as those enjoyed by participants in the ECAD and VLSI Design Skills initiatives are to be available. Experience in other countries has shown that, if this aim is to be achieved, it is essential to arrange nationwide co-operation in a co-ordinated action.