MICROELECTRONICS SENSOR ARRAYS WITH INTEGRAL PROCESSING CAPABILITY

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A 'smart' image sensor is described which is capable of performing low-level pre-processing of image data in parallel with the sensing operation. The chip consists of an array of 32 x 32 image sensing and storage cells and associated output circuits. The array is able to capture an image and simultaneously store the current and previous frames on separate capacitors located within each pixel site. Having the storage capacitors integrated into the sensing cells overcomes problems due to parasitic capacitance on the output lines which in turn improves the signal-to-noise ratio. The photocharge generated in the photodiode sensors is sensed non-destructively using a buffer amplifier prior to being sampled onto the local capacitor. The charge on each capacitor is sensed in turn in the same manner prior to being dumped to the output line. The output circuitry consists of a parallel array of differential amplifiers and comparators. The amplifiers perform frame-differencing between the current and previous frames while the comparators are used for global thresholding. The frame-differencing and thresholding modes can be enabled and disabled independently. The chip has been fabricated in a 2.4 μm double-poly CMOS process and is intended for use as a front-end in motion detection applications. At present its operation is limited to the calculation of differences between two successive frames. Further development would be needed in order for the chip to be used as a motion detector, in particular the tasks of edge-detection and region classification would need to be implemented. Since the objective was to achieve motion detection in real-time it is intended that these operations should be performed in hardware. It is for this reason that the outputs from the 2-dimensional imaging array are presented in parallel.

1. Introduction

One of the simplest approaches for detecting motion is to compare between two image frames $f(x,y,t_i)$ and $f(x,y,t_j)$ taken at time t_i and t_j , respectively, on a pixel-by-pixel basis. One procedure for doing this is to form a difference picture DP (Jain, 1981). The DP is generated by placing a 1 in each pixel for which the corresponding pixels in the two frames (previous and current frames) being compared have an appreciable difference in graylevel characteristics. In other words, a DP between previous frame taken at time t_i and current frame taken at time t_j may be defined as

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$$DP_{ij}(x,y) = \begin{cases} 1 \text{ if } \left|f(x,y,t_i) - f(x,y,t_j)\right| > \Theta \\ 0 \text{ otherwise} \end{cases}$$

where Θ is a threshold.

The above operation can be split into 2 parts, which are the subtraction phase and the comparison phase. Each of these operations is performed on a pixel-by-pixel basis, which means repetition operations covering all the pixels on the picture frame. For example, an image size of 575 x 525 pixels with 8-bit resolution will need 4.8 million subtraction and comparison bit-operations to produce a thresholded DP. For a real-time application, where each frame should be processed as it occurs, such a large number of operations has to be finished within 40 msec for a typical frame rate of 25 frame/second. Execution of a single such operation requires typically from several seconds to several minutes on conventional general purpose computers (Sherdell, 1980). Such intensive computational operations, therefore, are beyond the capability of a conventional single processor computer if the objective is to process image data in real time.

It is, therefore, necessary to use a real-time hardware solution to achieve real-time processing. The real-time hardware can process the image frame as it is scanned, and then pass the processed image to the next step. The final processed image can then be stored directly to the memory of the host computer for further processing. This has the additional advantage of omitting the need for a frame-grabber which takes time, adds to the system complexity and can be expensive. Although the implementation of general-purpose hardware architectures can be a complex and expensive task, a case can be made simpler by implementing some simple operations in dedicated hardware (Lee and Aggarwal, 1990).

Two types of solid-state imaging devices most commonly used in a number of application fields are charge-coupled device (CCD)-type and MOS-type (Tanaka et al, 1989). In the CCD-type device, reset noise is the major noise source, while switching noise and random noise due to high output impedance are the major noise sources in the case of the MOS-type device (Kyomasu, 1991). In this work, the second device in the form of a photodiode array has been chosen, mainly due to its simplicity of fabrication, which can use a conventional MOS process. In addition, the application does not need to achieve television picture resolution, which normally requires a small size for basic cell in order to accommodate a large number of cells in an array.

The main goal of this work is to produce a compact and simple real-time image processor array that could not only capture an image and store it, but also perform frame-differencing between successive frames and threshold the DP.

Section 2 describes the basic cell design concept, whereas the third section deals with alternative basic cell configurations. Section 4 explains the overall chip organisation. Section 5 deals with the layout considerations and the last section concludes the paper.

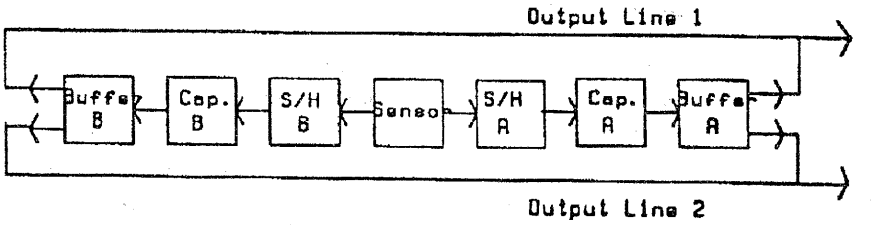

Fig. 1. Basic cell configuration.

2. Basic Cell Design Concept

As shown in Figure 1, the cell consists of a photodiode as an image sensor, sampling units, capacitors as memory units and buffers. Having local capacitors on each cell instead of in a separate memory array, overcomes problems due to parasitic capacitance on the output lines, which in turn will improve the signal-to-noise ratio. The input signal is the light intensity incident on the photodiode. In general, the cell operation consists of sensing, sampling and reading. The light sensing is done via a reverse-biased photodiode, which is reset periodically to a fixed voltage.

The photodiode collects the photogenerated electrons and discharges in proportion to the integration period and the photocurrent. At the end of the integration period, a sample-and-hold (S/H) unit reads the photodiode charge and transfers it onto a capacitor. Note that during even sample periods the S/H_A will transfer the photodiode charge onto the capacitor C_A, while the S/H_B will be disabled to allow the charge on capacitor C_B to be dumped onto the first output line, which represents the previous frame, through buffer B. At the same time as the charge on capacitor C_B is being dumped (just after the photodiode charge has been sampled), the charge on capacitor C_A can also be dumped to the second output line, which represents the current frame. Due to the nondestructive method applied on reading the storage capacitors, this reading operation can be done once again at odd sample periods. In turn, the S/H_B will transfer the photodiode charge onto capacitor C_B during odd sample periods. The S/H_A will be disabled during these periods. Just after the S/H_B samples the photodiode charge, the charge on capacitor C_B will be dumped to the second output line, while the charge on capacitor C_A will be dumped to the first output line. It is clear, therefore, that each of the output lines is connected to both buffers in turn.

The voltages across the capacitors follow or proportionally follow the voltage across the photodiode, depending on the S/H circuit used in the cell. It can be either a voltage follower or a switch transistor that transfers the charge stored in the photodiode depletion capacitance onto the capacitor C_A or C_B. In the latter case, the capacitors should be precharged to a starting voltage prior to the sampling.

The cell size should be minimised in order to achieve higher resolution. Therefore, only N-type transistors were used in the cell, although the chip was fabricated using a CMOS technology.

3. Alternative Basic Cell Configurations

To achieve optimum performance from the chip, the best cell configuration and layout is the key factor. The S/H in Figure 1 can be implemented in two ways either by using only pass transistors or by using a buffer in a source-follower configuration.

Figure 2 shows the cell configuration obtained by incorporating pass transistors in place of S/H_A and S/H_B in Figure 1. At the beginning of a sample period, the photodiode will be precharged to (V_{DD} - $V_{threshold}$) and both output lines will be discharged to V_{SS}, this being controlled by signal CT_1. Capacitor C_A (or C_B) will be precharged to the same value as the photodiodes at the beginning of every even (or odd) sample period, which is controlled by signal CT_{2A} (or CT_{2B}). At the end of every even (or odd) integration period, a fraction of the photodiode charge will be transferred to capacitor C_A (or C_B) through pass transistor $M2_A$ (or $M2_B$). During even sample periods, just after charge-sharing between the photodiode and capacitor C_A has finished, signal CT_{3A} will read the voltage output on buffer A to the first output line (current frame) and the voltage output on buffer B to the second one (previous frame). At odd sample periods, just after the transfer of a fraction of photodiode charge to capacitor C_B finished, signal CT_{3B} will read the voltage output on buffer B to the first output line and voltage output on buffer A to the second one.

There are certain disadvantages associated with this configuration. It needs 7 control signals which makes it rather complicated to implement. Two extra control signals are needed to precharge both capacitors. Destructive sensing accomplished by means of charge-sharing between the photodiode and the capacitor means that the voltage across the capacitor will be much less than the one across the photodiode. This can be clearly seen in the simulation results obtained using simulated photodiode voltages.

This situation occurs due to the capacitance of the photodiode being much smaller than that of the capacitors. Typical capacitance of 784 μm^2 p - n+ junction photodiode at zero bias is 36.8 fF. In contrast, the capacitance of 345 μm^2 polyl -poly2 capacitor is 218 fF. It is easy to show, therefore, that the voltage across the capacitor will only be 15% of the original voltage across the photodiode.

By placing a buffer between the photodiode and the pass transistors, the two extra control signals can be eliminated while maintaining the number of transistors used in the cell. The circuit diagram for this basic cell is shown in Figure 2. In addition, the voltage across the capacitors is degraded only by the threshold voltage of the N-type transistor in the buffer.

The only disadvantage of this configuration is the fact that the output voltages are degraded by a double threshold voltage drop due to the 2 stages of buffering that are used. But this problem can be overcome by controlling the light intensity incident on the photodiode.

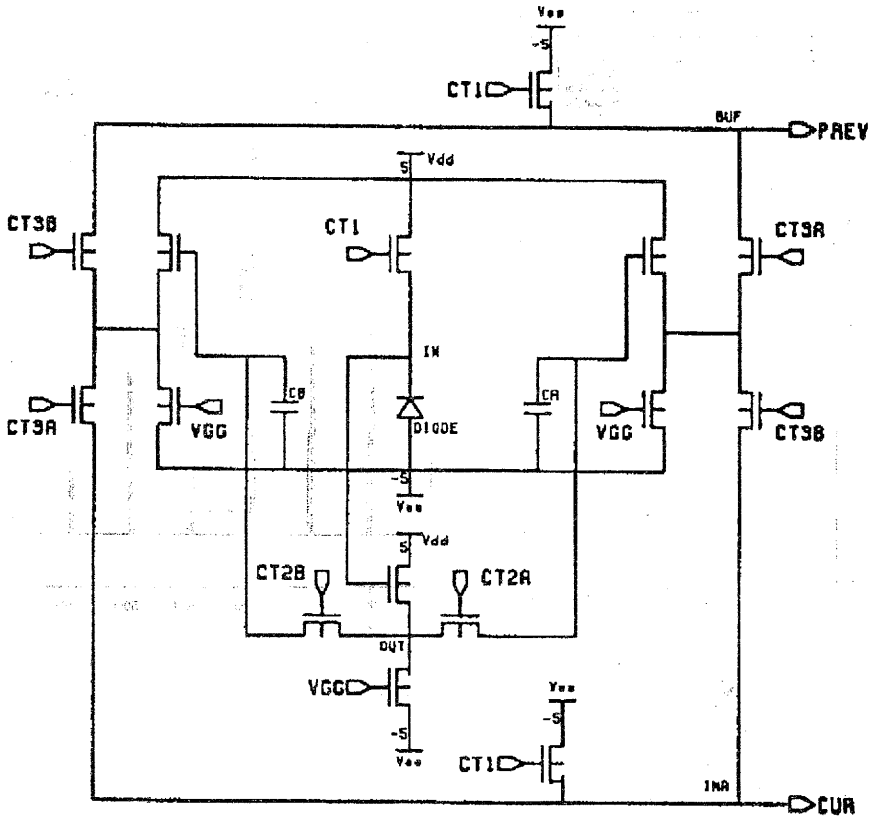

Fig. 2. The basic cell with double buffer stages.

The simulation results are shown in Figure 3. The point of interest is the voltage difference between the current and previous frames. The difference has to be kept as small as possible in order to get a good result. Figure 3 shows that the difference becomes bigger as the sample period increases. This indicates that the capacitors are self-discharging. This problem can be overcome either by increasing the frame-rate or by making the capacitor bigger. To maintain a minimum size for the cell, the only option for this problem is increasing the frame-rate.

The next consideration in designing the cell after implementation of the S/H is to design the control signals scheme. With 5 control signals excluding the power supply which have to be connected in the array, it is difficult to implement and difficult to maintain a minimum size for the cell. A large portion of the silicon area between cells will be occupied by the signal connections which in turn will lower the spatial resolution of the image sensor due to greater distance being required between adjacent cells.

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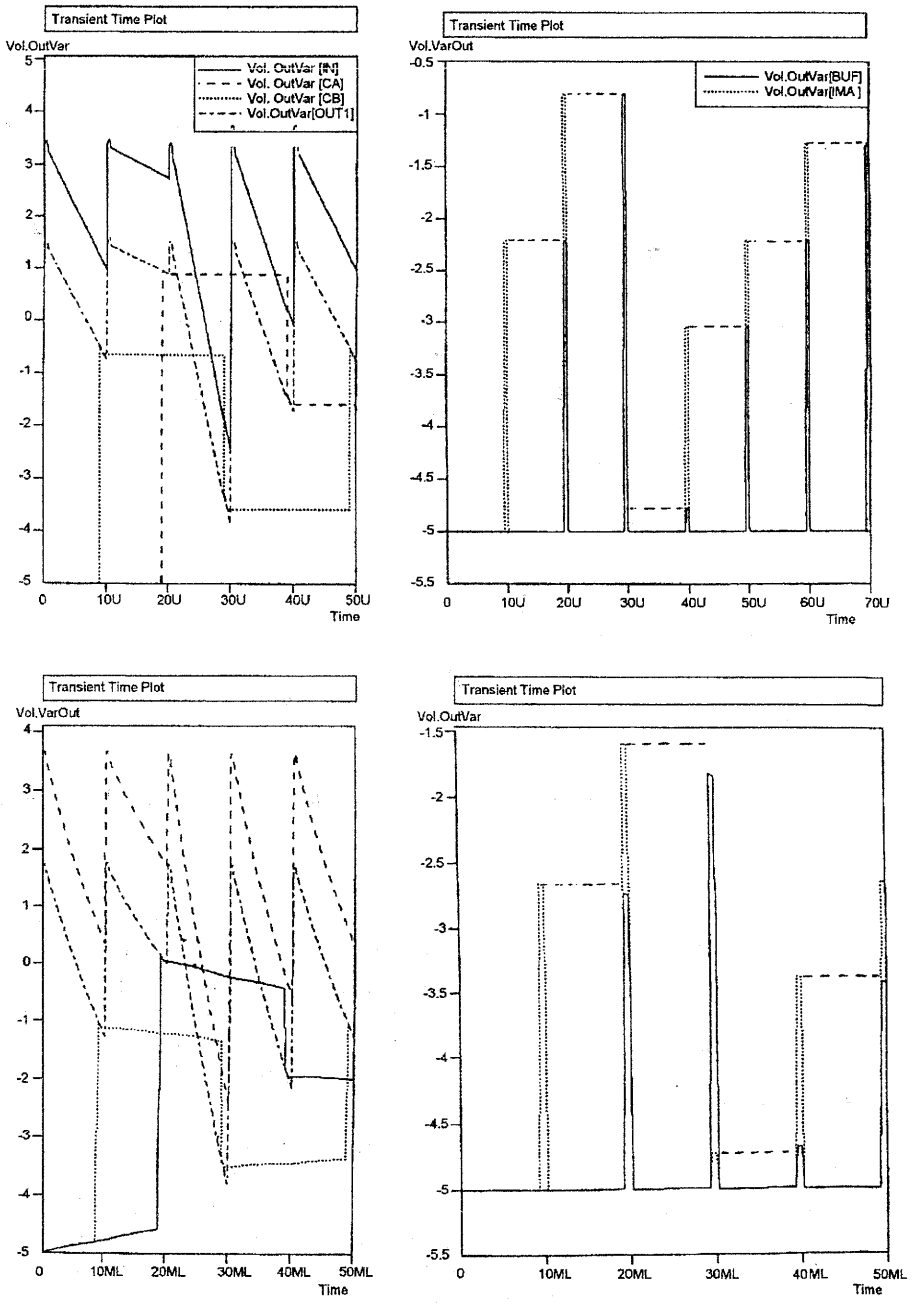

Fig. 3. The simulation results for basic cell in Fig. 2.

Further reduction of the number of control signals can only be achieved by eliminating the control signals CT_{3A} and CT_{3B} in Figure 2 and replacing them by control signals CT_{2A} and CT_{2B}, respectively. In this case, the sensing and reading operations will occur at the same time. Nevertheless, this does not significantly affect the results (Figure 4) due to the nondestructive sensing method used. In other words, the voltage difference observed between current and previous frames shown in simulation results in Figure 4 is still in the tolerance range.

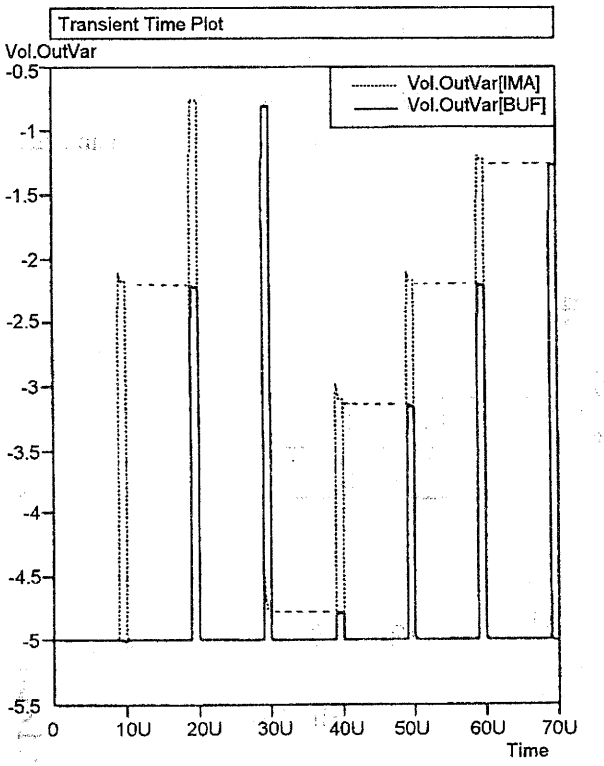

Fig. 4. Simulation results of basic cell with 3 control signals.

4. The Chip Organisation

The chip consists of a 32 x 32 array of basic cells, three shift registers and output circuits arranged in a parallel configuration. The outputs were left in parallel for further future development. Figure 5 shows the overall chip structure. The shift registers are used to shift the control signals from one column to the next right one. The output lines of cells belonging to the same row share common output lines as indicated in Figure 6.

Readout is done in parallel, starting from the first column, which is the most left one. The signals Φ1 and Φ2 of the shift register control the shifting of the readout sequence.

The output circuits basically consist of differential amplifiers for frame differencing and comparators for global thresholding. The threshold value can be adjusted through a Thres signal to achieve the best result. To add flexibility to the design, the frame differencing and thresholding functions can be disabled independently by means of Model and Mode2 signals, respectively. Therefore, the four possible modes available for this design are as follows:

- Unthresholded DP if both signals at model and mode2 are high.
- Thresholded DP if model signal is high and mode2 signal is low.
- Unthresholded Current Frame if model signal is low and mode2 signal is high.
- Thresholded Current Frame if both signals at model and mode2 are low.

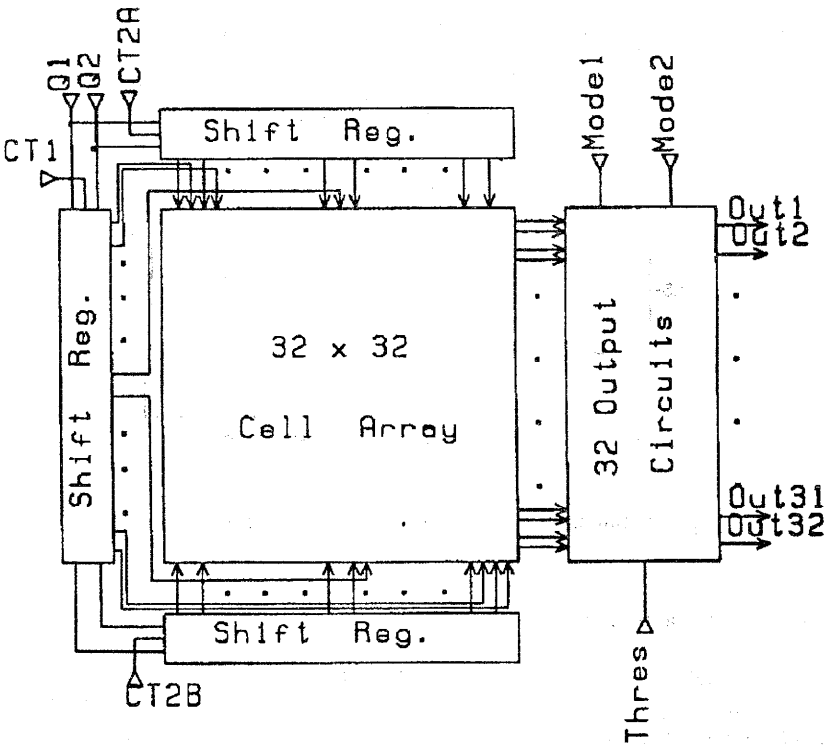

Fig. 5. The overall chip structure.

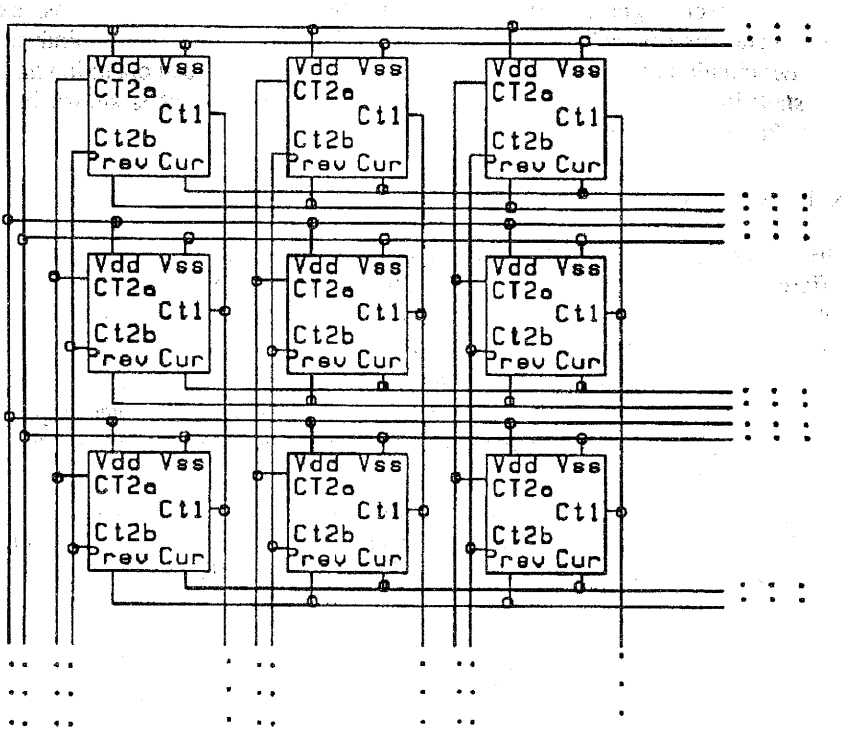

Fig. 6. Interconnections between adjacent cells.

5. The Layout Considerations

A quarter of the basic cell area is occupied by the photodiode and two capacitors. The photodiode lies in the centre of the cell and has a square shape. The cell has also a square shape in order to keep the same distance between adjacent cells. The photodiode size is 28 μm x 28 μm, while the capacitors size is 9.6 μm x 36 μm. The overall cell size is 92.4 μm x 92.8 μm. All the switch transistors are minimum size for the given technology. The photodiode is an p - n+ source/drain diode with total capacitance of about 36.8 fF at zero bias. This capacitance decreases as the diode voltage increases. The capacitors were designed to have sufficiently large capacitance in order to reduce self-discharge effect at lower frame rates. Their capacitance of 218 fF is sufficient to prevent self-discharge less than 1 % for frame rates of greater than 25 frame/second according to the simulation results. The capacitors are implemented by putting poly2 layer on top of poly1.

Simple mirroring techniques were used for connecting adjacent cells, in the interest of keeping the cell size small. All four signal lines (V_{DD}, V_{SS}, V_{GG} and Buffro / Previous Frame) at the outside edges of a cell will share with the ones in adjacent cells.

To prevent light penetrating to other diodes, all the active areas, except the photodiode, are covered by the metal layer. This light may cause photoinduced current in other circuit nodes. Those currents may interfere with the cell operation and result as crosstalk in other cells (Pecht et al, 1991). The output circuit is shown in Figure 8, while Figure 7 shows the overall chip layout.

6. Conclusions

The design of a dedicated VLSI chip for real-time image capture and frame differencing has been described. It is intended to be used as a front end in motion detection applications based on background differencing between two successive-frames. The chip is being tested at the time of writing.

The chip can perform frame differencing between two successive frames and global thresholding. In addition, these functions may be disabled separately and independently, resulting in four modes of output : the thresholded and unthresholded DPs as well as the thresholded and unthresholded current frames.

Each cell consists of a photodiode, two identical capacitors, switching transistors and 2-stage buffers. Several configurations of basic cell were discussed and simulated. A chip consisting of a 32 x 32 cell array based on the preferred cell configuration and

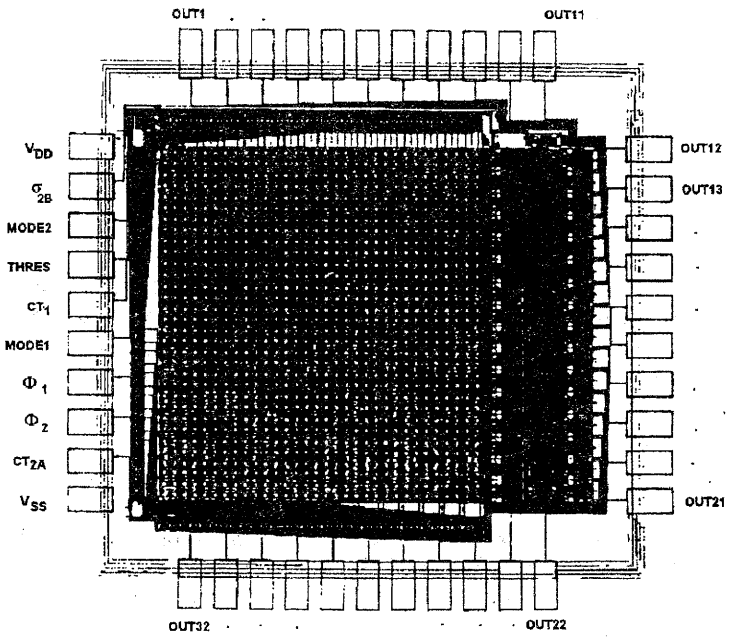

Fig. 7. The chip layout.

Fig. 8. The output circuit layout.

its associated output circuits has been fabricated in a 2.4 μm double-poly CMOS process.

The readout, frame-differencing and thresholding operations are done in a highly parallel manner to facilitate real-time image processing. The final output lines were left in parallel for further development in the future.

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